ABSTRACT OF THE DISCLOSURE

In a bit-line direction, a plurality of memory mats are arranged including a plurality of memory cells respectively coupled to bit lines and word lines, and a sense amplifier array is arranged including a plurality of latch circuits having input/output nodes connected to a half of bit-line pairs separately provided to the memory mats in a region between the memory mats placed in the bit-line direction, thereby making possible to replace with a redundant bit line pair and the corresponding redundant sense amplifier on a basis of each bit-line pair and sense amplifier connected thereto, thereby realizing effective and rational Y-system relief.